REMARKS

Claims 1, 2, 5-8, 11, 12, 15 and 17-24 are now pending in the application, with claims 1 and 7 being the independent claims. Reconsideration and further examination are respectfully requested.

In the Office Action, claims 1 and 7 were rejected under the judicially created doctrine of obviousness-type double patenting over claims 1 and 14 of U.S. Patent No. 7,093,147 (the '147 patent). Specifically, it is asserted in the Office Action that "the plurality of computer processing jobs in claims 1 and 7 of the instant application is equivalent to the running of the software in claims 1 and 14 of U.S. Patent No. 7,093,147" and that "the 'best fit' limitation (in view of its description on the Specification) in claim 1 of the instant application is contained in the comparison and selection of the processing core to run the software." In response, it is noted that independent claims 1 and 7 have been amended above and now recite that computer processing jobs are moved or transferred "to improve a throughput metric", rather than "according to a best fit of processor hardware availability to processing software requirements" (as was previously recited). There is nothing in the claims of the '147 patent that would have suggested or motivated one of ordinary skill in the art to move or transfer computer processing jobs among computer processor cores to improve a throughput metric. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 16 was rejected on the ground of nonstatutory obviousness-type double patenting over claim 1 of the '147 patent in view of US Patent Application Publication No. 2003/0110012 (Orenstien). However, the cancellation of claim 16 above is believed to have rendered this rejection moot.

Claims 1-16 were rejected under 35 U.S.C. § 102(e) over Orenstien. Withdrawal of this rejection is respectfully requested for the following reasons.

The present invention concerns systems, methods and techniques for improving computer system processing performance. In the preferred embodiments, multiple different kinds of processor cores are provided and computer processing jobs are moved or transferred among them in order to improve a throughput metric.

In particular, independent claim 1 is directed to a computer system that includes multiple computer processor cores in which at least two differ in processing performance, and in which all execute the same instruction set. The computer system also includes a performance measurement and transfer mechanism that moves a plurality of executing computer processing jobs amongst the computer processor cores to improve a throughput metric.

Independent claim 7 is directed to a method for operating multiple processor cores, in which multiple computer processor cores are placed on a single semiconductor die, in which at least two computer processor cores differ in processing performance, and in which all execute the same instruction set. Performance is measured for each of a set of computer processing jobs hosted amongst the plurality of computer processor cores, and individual ones of the computer processing jobs are transferred amongst targeted ones of the computer processor cores to improve a throughput metric.

Both of independent claims 1 and 7 have been amended above to clarify that the computer processing jobs are moved or transferred among the processor cores to improve a throughput metric. This feature of the invention is supported in the Title and at page 1 lines 10-14, page 2 lines 10-11, page 11 lines 14-24 and page 12 lines 17-22 of the Specification. Because this feature perhaps was not recited in the originally filed claims with adequate clarity, it

was not considered in the present Office Action. However, Orenstien has been studied in detail and is not seen to say anything at all about this feature of the invention. Rather, Orenstien only appears to discuss techniques for distribution of processes based on power-consumption and thermal considerations. Lacking this feature of the invention, Orenstien could not have anticipated independent claims 1 and 7, and so withdrawal of this rejection is respectfully requested.

The other rejected claims in this application depend from the independent claims discussed above, and are therefore believed to be allowable for at least the same reasons. Because each dependent claim also defines an additional aspect of the invention, however, the individual reconsideration of each on its own merits is respectfully requested. In addition, the newly added claims highlight other aspects of the present invention.

New claim 17 depends from independent claim 1 and recites the additional feature that at least one of an operating system hosted on the plurality of computer processor cores, firmware, and special-purpose hardware includes the performance measurement and transfer mechanism. This feature the invention is supported, e.g., at page 9 lines 11-17 and by original claims 2-6 and 8-12 of the Specification and, particularly in combination with the other features recited in claim 1, is not believed to be disclosed or suggested by the applied art.

New claim 18 depends from independent claim 1 and recites the additional feature that the performance measurement and transfer mechanism maximizes total system throughput. This feature the invention is supported, e.g., at page 2 lines 26-32, page 12 lines 2-6 and the Abstract of the Specification and, particularly in combination with the other features recited in claim 1, is not believed to be disclosed or suggested by the applied art.

New claim 19 depends from independent claim 1 and recites the additional feature that the performance measurement and transfer mechanism periodically transfers the executing computer processing jobs to a new assignment amongst the plurality of computer processor cores, collects performance statistics about execution at the new assignment, and then determines whether to reassign the executing computer processing jobs to different computer processor cores based on the performance statistics collected. This feature the invention is supported, e.g., at Figure 2, page 8 line 34 through page 9 line 10 and page 10 line 33 through page 11 line 24 of the Specification and, particularly in combination with the other features recited in claim 1, is not believed to be disclosed or suggested by the applied art.

New claim 20 depends from claim 19 and recites the additional feature that the performance measurement and transfer mechanism swaps execution of the executing computer processing jobs between the computer processor cores for a period of time, monitoring resulting performance, and then builds a table with relative performances of jobs on different types of cores. This feature the invention is supported, e.g., at page 9 lines 19-25 of the Specification and, particularly in combination with the other features recited in claims 1 and 19, is not believed to be disclosed or suggested by the applied art.

New claim 21 depends from claim 20 and recites the additional feature that the jobs are reassigned based on the relative performances, by assigning jobs that benefited most from large complex processor cores to said large complex processor cores. This feature the invention is supported, e.g., at page 9 lines 26-36 of the Specification and, particularly in combination with the other features recited in claims 1, 19 and 20, is not believed to be disclosed or suggested by the applied art.

New claim 22 depends from claim 19 and recites the additional feature that the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics. This feature the invention is supported, e.g., at page 5 lines 26-29 of the Specification and, particularly in combination with the other features recited in claims 1 and 19, is not believed to be disclosed or suggested by the applied art.

New claim 23 depends from independent claim 1 and recites the additional feature that the throughput metric comprises a number of instructions per second. This feature the invention is supported, e.g., at page 4 lines 31-35 and page 9 lines 17-19 of the Specification and, particularly in combination with the other features recited in claim 1, is not believed to be disclosed or suggested by the applied art.

New claim 24 depends from independent claim 1 and recites the additional feature that movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals. This feature the invention is supported, e.g., at page 13 lines 25-28 of the Specification and, particularly in combination with the other features recited in claim 1, is not believed to be disclosed or suggested by the applied art.

In order to sufficiently distinguish Applicants' invention from the applied art, the foregoing remarks emphasize several of the differences between the applied art and Applicants' invention. However, no attempt has been made to categorize each novel and unobvious difference. Applicants' invention comprises all of the elements and all of the interrelationships between those elements recited in the claims. It is believed that for each claim the combination of such elements and interrelationships is not disclosed, taught or suggested by the applied art. It

is therefore believed that all claims in the application are fully in condition for allowance, and an indication to that effect is respectfully requested.

If there are any fees due in connection with the filing of the currently submitted papers that have not been accounted for in this paper or the accompanying papers, please charge the fees to Deposit Account No. 08-2025. If an extension of time under 37 C.F.R. 1.136 is required for the filing of any of the currently submitted papers and is not accounted for in this paper or the accompanying papers, such an extension is requested and the fee (or any underpayment thereof) should also be charged to the Deposit Account.

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